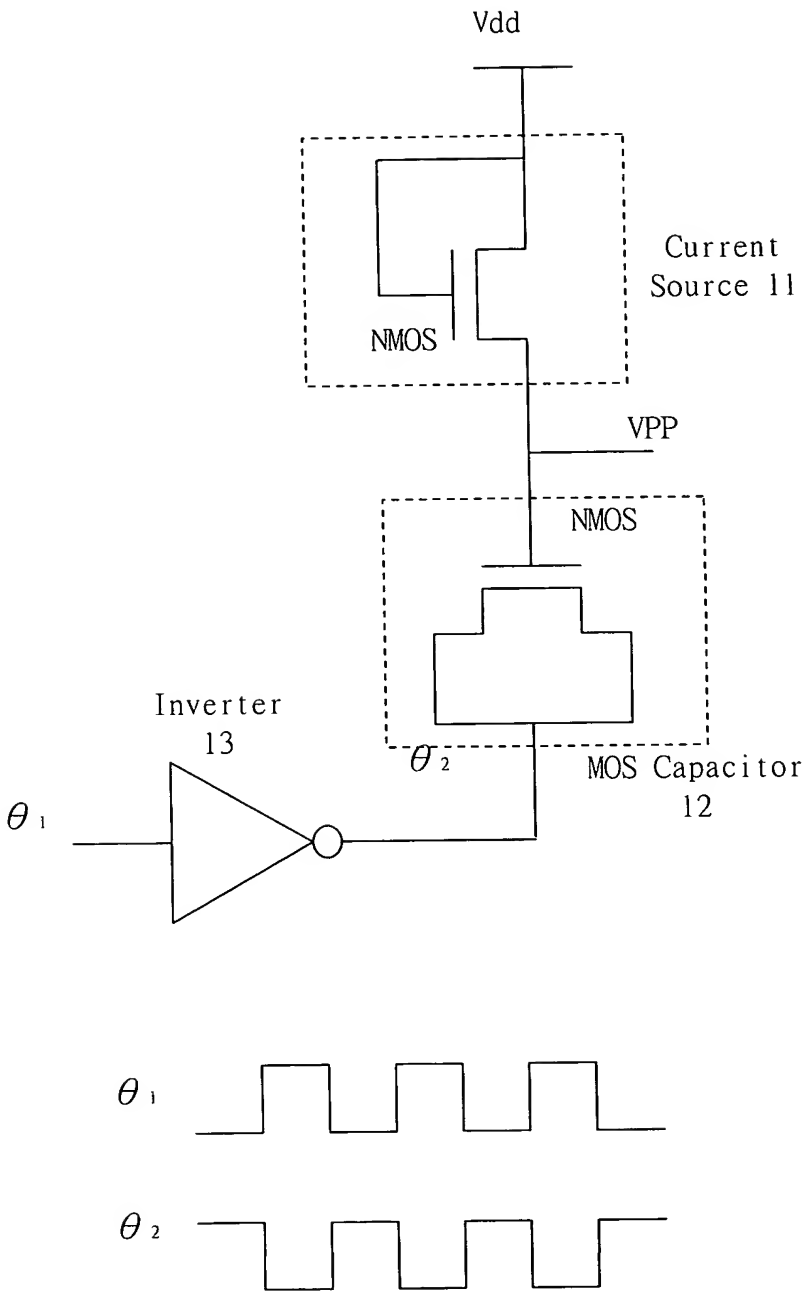

Figure 1 (Prior Art)

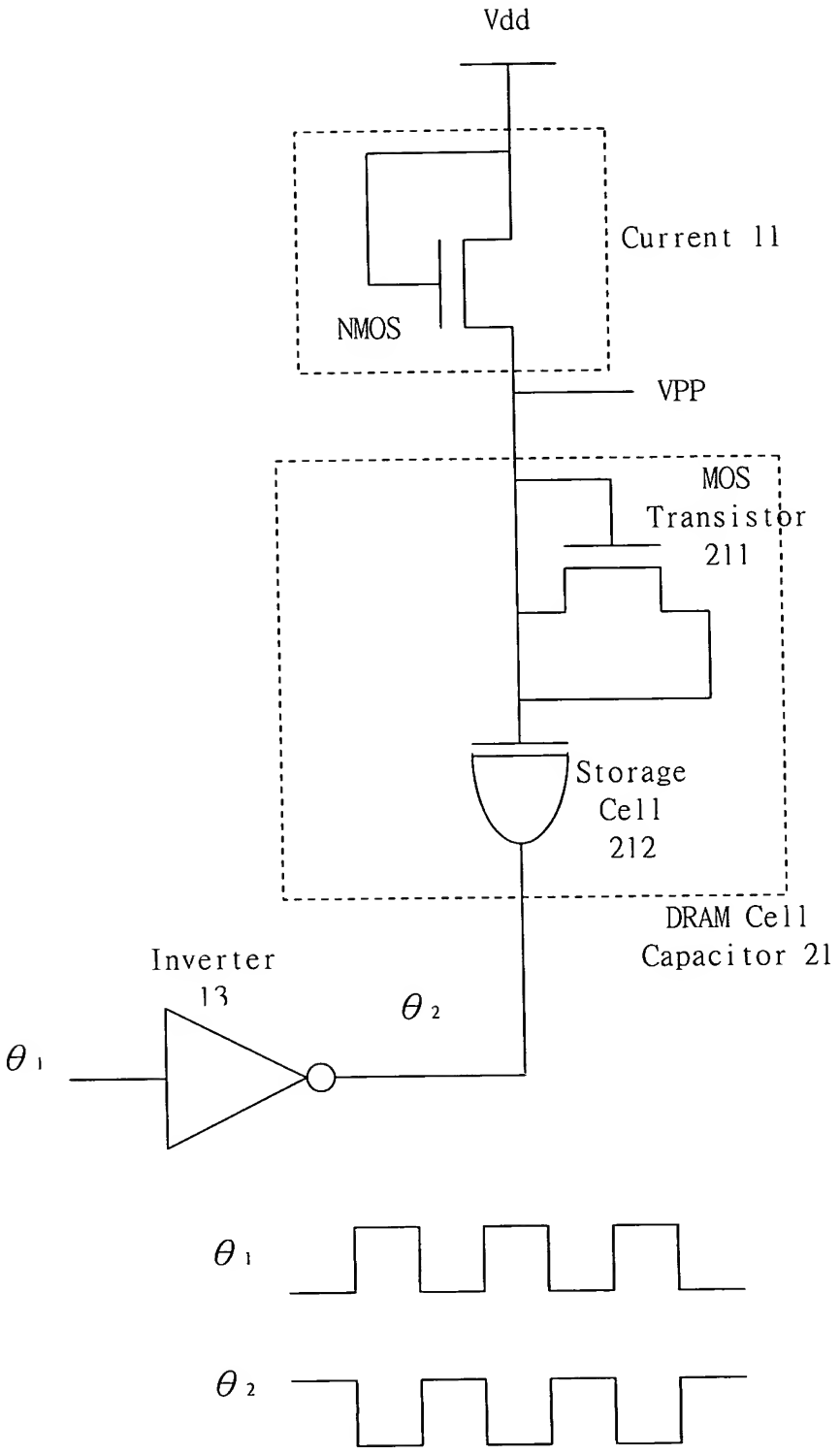
Vdd
Current 11
NMOS
VPP
MOS
Transistor
211
Storage
Cell
212
DRAM Cell
Capacitor 21
Inverter
13
θ2
θ1
θ1
θ2

Figure 2(A)

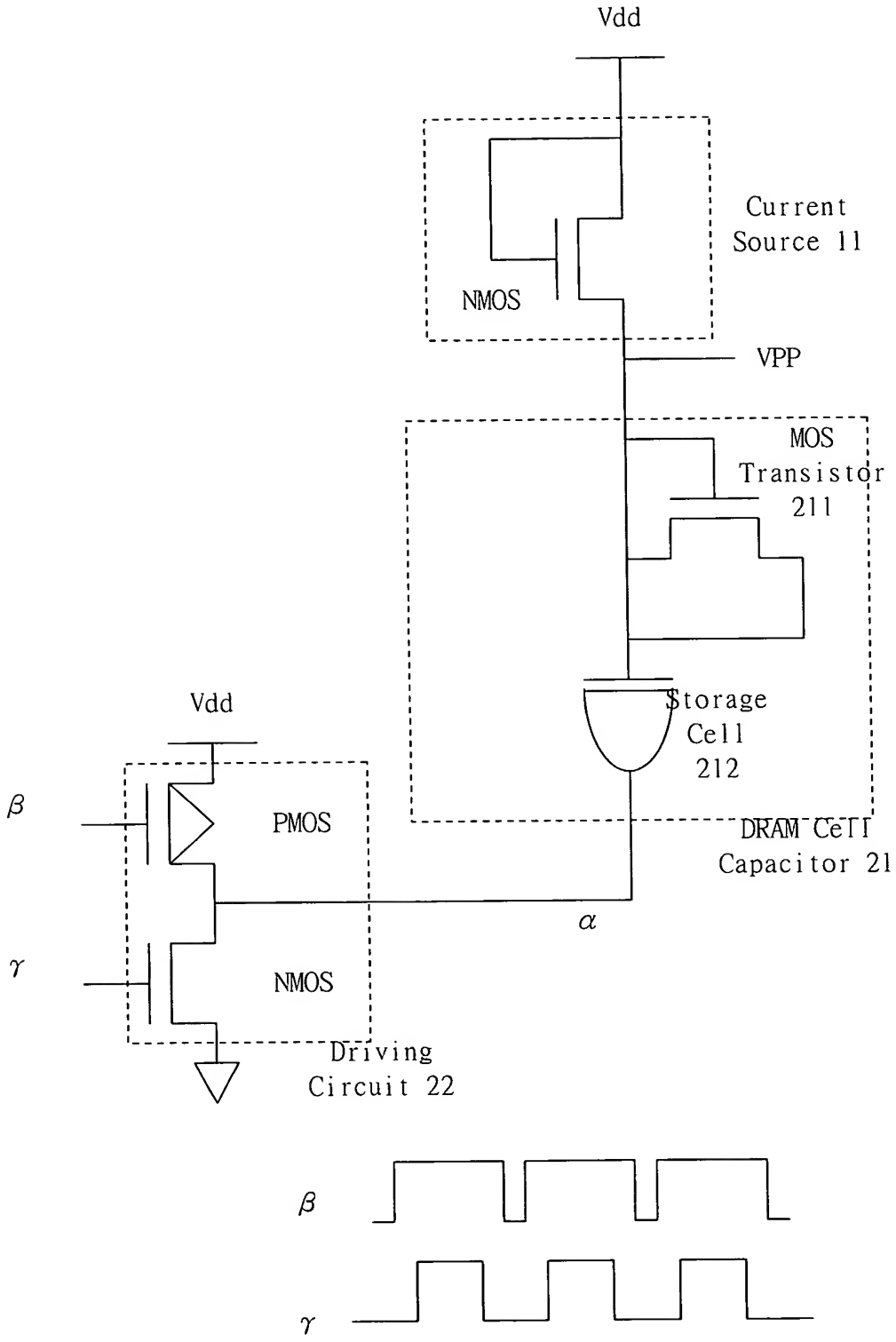
Vdd
Current
Source 11
NMOS
VPP
MOS
Transistor
211
Storage
Cell
212
DRAM Cell
Capacitor 21
Vdd
β
PMOS
α
γ
NMOS
Driving
Circuit 22
β
γ

Figure 2 (B)